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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
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| | 09/602,938 | MOORE, MICHAEL T. | |
| | Examiner | Art Unit | |
| | William P Moore | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 to 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 to 20* is/are rejected.

7)☒ Claim(s) *1, 4-9, 11, 12, 15, 16, 18, 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2000* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☒ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

# Detailed Office Action

## *Specification*

1. The disclosure is objected to because of the following informalities:

(a) On page 5, line 4, please change "600" to "800".

(b) On page 5, line 9, please correct grammar "It would desirable".

(c) On page 8, line 17, please correct grammar "may in".

(d) On page 11, line 1, please change "402" to "410".

## *Drawings*

2. Fig 4A and 4B are objected to because they do not label the memories as first and second non-volatile memories as referred to in Fig 5, steps 502 and 503 and in the specification page 12, para. 5.

3. Figure 4 is objected to because it does not label BIST data with number 408 as used in specification on page 12, line 11.

4. Figs 6A, 6B, and 6C are objected to because the dashed area is not labeled as Nonvolatile elements as described in specification on page 12, line 20.

## *Claim Objections*

5. Claim 1 to 9, 11, 12, and 16 are objected to because they contain grammatical informalities.

(a) In claim 1, please change "store" to read "storage means".

(b) In claim 4, please change "store" to read "storage means".

(c) In claim 5, please change "store" to read "storage means".

(d) In claim 6, please change "store" to read "storage means".

(e) In claim 7, please change "store" to read "storage means".

(c) In claim 8, please change "store" to read "storage means".

(d) In claim 9, please change "store" to read "storage means".

(e) In claim 11, please change "store" to read "storage means".

(f) In claim 12, please change "store" to read "storage means".

(g) In claim 16, please change "store" to read "storage means".

(h) In claim 16, please change "store" to read "storage means".

(i) In claim 18, please change the phrase "that places a programmable logic circuit" to read: ", said information for placing said programmable logic circuit".

(j) In claim 16 please insert "on" before "one die".

(k) In claim 15 please insert "storage means" after "self-test nonvolatile".

(l) In claim 20 please change "than" to "from".

***Claim Rejections - 35 USC 103***

*Statement of Statutory Basis*

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

*Claim 1*

7. Claim 1 is rejected under 35 U.S.C 103(a) as being unpatentable over Stroud et al. (US Patent 5,991,907) in view of Kang et al. (US Patent 5,889,701), further in view of Pathak et al. (US Patent 5,946,267).

Stroud et al. has disclosed a programmable logic device assembly (*see*, fig. 1 disclosing the architecture of a FPGA, i.e. a programmable logic device) , comprising:

a programmable logic circuit that provides functions according to configuration data including a self-test function (*see*, col. 4, lines 6-9, disclosing that programmable logic circuit is programmed for diagnostic testing, i.e. self-testing); and

at least one storage device coupled to the programmable logic circuit that provides self-test configuration data for the programmable logic circuit and can subsequently store user configuration data (*see*, col. 4, lines 47-49, disclosing that self-test configuration data, i.e. BIST configuration, is stored in the test

controller; *see*, id., col. 2, lines 15-20, disclosing that the programmable logic device, i.e. FPGA, is temporarily programmed. This suggests that the FPGA is later reprogrammed with user configuration data. Also, an FPGA is not useful unless it is eventually programmed with user configuration data. That is, programming the FPGA with only test configuration data and never loading user configurations is not a useful function for a FPGA.).

One difference between the claim and Stroud et al., is that Stroud et al. is silent about whether the storage device used to hold the self-test configuration data is non-volatile. This difference is overcome by an obvious modification of Stroud et al. in view of Kang et al., and further in view of Pathak et al.

Kang et al has disclosed that an In-System Programmable device (ISP) is a device that can be programmed, erased, and verified after it has been connected, such as by soldering, to the system printed circuit board. *See*, Kang et al., col. 1, lines 23-26.

Kang et al. has further disclosed that an ISP programmable logic device (PLD) has the advantage of not requiring special test equipment external to the system in order to configure the PLD. *See*, col. 1, lines 26-28.

Combination A

At the time of invention it would have been obvious for a person of ordinary skill in the art to replace the programmable logic device of Stroud et al. with an equivalent programmable logic device with ISP capability, where ISP capability was disclosed by Kang et al..

The motivation for doing so would be to provided the advantage of allowing the programmable logic device to be tested in-system without requiring external test equipment. *See*, Kang et al., col. 1, lines 26-38.

Pathak et al. has disclosed a serial configuration memory for in-system configuration of programmable logic devices, see col. 1, lines 40-63, and col. 1, lines 10-19. Pathak et al. suggests that a serial configuration memory is conventionally a non-volatile memory, see col. 1, lines 20-25.

Combination B

At the time of invention it would have been obvious for a person of ordinary skill in the art to modify the combination of Stroud et al. and Kang et al. such that the programmable logic device with ISP capability is configured in-system using the serial configuration memory of Pathak et al.. This modification realizes as obvious the claim limitation of a non-volatile memory device coupled to the programmable logic device.

The motivation for making this modification would be to provide high speed configuration of the programmable logic device in-system, see Pathak et al., col. 1, lines 51-52.

*Claim 2*

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Stroud et al., Kang et al., and Pathak et al. (combination B) as applied to claim 1 above.

The combination of Stroud et al., Kang et al., and Pathak et al. (combination B) has disclosed that the programmable circuit can provide a self-test result (pass/fail flag) when configured for self-test function. *See*, Stroud, col. 2, 44-60 (disclosing the step of analyzing the results of the self-test to produce a pass/fail indication).

*Claim 3*

9. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Stroud et al., Kang et al., Pathak et al., (combination B) as applied to claim 1 above, further in view of Lawman (US Patent 6,044,025 A).

The combination of Stroud et al., Kang et al., Pathak et al. (Combination B) is silent about the use of a test port for providing the self-test results in a predetermined format.

Lawman has explicitly disclosed a test port for the purpose of self-test for in-system configuration of a programmable logic device. Lawman has disclosed a method of In-System Programming, whereby a test access port (a JTAG 1149.1 boundary scan TAP) is used for transmitting configuration data to a programmable device after the device is mounted onto a PCB. Further, Lawman has disclosed the use of a test port for programming as a built in feature for an off-the-shelf FPGA. (*see*, Lawman et al., col. 1, lines 22-54)

Combination C

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify Stroud-Kang-Pathak such that the programmable logic device with ISP capability is a standard off-the-self FPGA that is in-system programmable by way of a built in test port as disclosed by Lawman.

The motivation for doing so is because use of a test-port is conventional for in-system programming of programmable logic devices, and also because off-the-shelf parts are less expensive. (*see*, Lawman et al., col. 1, lines 22-54)

*Claim 4*

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Stroud et al., Kang et al., Pathak et al., (combination B) as applied to claim 1 above, further in view of Shyu (US 6,046,957 A).

The combination of Stroud et al., Kang et al., Pathak et al. (Combination B) has not disclosed that the first nonvolatile storage device is formed with the programmable logic circuit on a single integrated circuit die.

Shyu has disclosed that with the growing trend toward SOC (system-on-a-chip) technology, it is inevitable to incorporate a variety of circuit building blocks, each performing a specific function of an electronic system, onto a single integrated circuit chip. Shyu further discloses that memory devices are usually needed in a system chip. Generally, many memory macros will be embedded within the system chip that commands these memories. The embedded memory macros may be volatile, such as SRAM and DRAM, or non-volatile, such as mask ROM, EPROM, EEPROM and flash memory, and can have parts that differ much in configuration from the standard stand-alone memory devices. (*see*, col. 1, lines 10-28)

Combination D

At the time of invention it would have been obvious for a person of ordinary skill in the art to modify the combination of Stroud et al., Kang et al., Pathak et al. (combination B), such that the nonvolatile storage device and the programmable logic device are formed together on the same die as suggested by Shyu.

The motivation for doing so is because increasing circuit integration is a well known technological trend. Also, examiner takes official notice that it is old and well known that system-on-a-chip designs provide the advantage of reduced power consumption and allow faster bus communications speeds as compared to systems comprising a plurality of individual integrated circuits.

*Claim 5*

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Stroud et al., Kang et al., Pathak et al., and Shyu, (combination D) as applied to claim 4 above, further in view of Snowden et al. (US 4,771,399 A).

The combination of Stroud et al., Kang et al., Pathak et al., and Shyu (combination D) has not disclosed that the first nonvolatile storage device includes re-programmable nonvolatile circuit elements.

However, the combination of Stroud et al., Kang et al., Pathak et al., and Shyu (combination D) has disclosed that the first nonvolatile storage device is a Programmable ROM (PROM). It is old and well known that a PROM is a memory device that is programmable only once.

Snowden et al. has taught that an electrically erasable memory (EEPROM) has the advantage of re-programmability as compared to PROM memories. That is, an EEPROM can be programmed more than once. (Col. 1, lines 45-62).

Combination E

At the time of invention it would have been obvious for a person of ordinary skill in the art to modify the combination of Stroud et al., Kang et al., Pathak et al., and Shyu (combination D) such that the PROM is redesigned as an EEPROM, as suggested by Showden et al.

One of ordinary skill in the art would have recognized that this would allow the BIST and user configuration data to be changed in the field without needing to remanufacture the integrated circuit. Thus, One would have been motivated to make this change in order to provide the benefit of re-programmability to the non-volatile memory. (Showden et al., col. 1, lines 45-62)

*Claim 6*

12. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Snowden et al., as applied to claim 5 above.

The combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Snowden et al. (Combination E) has disclosed that the first nonvolatile storage device includes electrically erasable programmable read-only-memory cells. (See rejection of Claim 5 under 35 U.S.C 103(a), combination E).

*Claim 7*

13. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the combination of Stroud et al., Kang et al., Pathak et al., and Shyu, (combination D) as applied to claim 4 above, further in view of Cook (A First Course in Digital Electronics, Prentice-Hall 1999, page 684-689).

The combination of Stroud et al., Kang et al., Pathak et al., and Shyu (Combination D) has not explicitly disclosed that the self-test configuration data in the one nonvolatile storage device is set by at least one manufacturing process step.

The combination of Stroud et al., Kang et al., Pathak et al., and Shyu (Combination D) has disclosed that the nonvolatile storage device is a programmable ROM (PROM) that is programmable only once. (See Pathak et al.)

Cook has disclosed a Mask Programmable ROM (MROM) that is a read-only memory in which the manufacturer generates a photographic negative or mask designed to store the customer-specification data requirements. Mask programmable ROMs or MROMs are permanently programmed by the manufacturer by simply adding or leaving out diodes or transistors, as previously shown. (*see*, Cook, page 684)

Cook has further taught that MROMs have a cost advantage over PROMs when a device is mass produced. (*see*, Cook, page 684).

Combination F

At the time of invention it would have been obvious for a person of ordinary skill in the art to modify the combination of Stroud et al., Kang et al., Pathak et al., and Shyu (Combination D) such that the PROM is replaced by an equivalently functional MROM, as suggested by Cook.

The motivation for doing so would be to mass produce the device at low cost. (Cook, page 684)

*Claim 8*

14. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of of Stroud et al., Kang et al., Pathak et al., Shyu, and Cook (combination E), as applied to claim 7 above.

The combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Cook (Combination F), has disclosed a nonvolatile storage device includes a mask programmable read only-memory that stored self-test configuration data (*See* obvious rejection of claim 9 under 35 USC 103(a), combination F, MROM)

The combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Cook (Combination F), has not explicitly disclosed a separate memory that can store user configuration data (this memory corresponds to the SRAM.cells of the programmable logic device, FPGA, that stored the current configuration of the programmable logic device, either self-test or user configuration. These configurations are provided from the MROM to program the SRAM cells of the programmable logic device).

One of ordinary skill in the art would have recognized that the self-test configuration only needs to be changed during the initial system design prototyping of the programmable logic device, whereas the user configuration data depends on the application that the user decides to use the FPGA for.

Combination N

At the time of invention it would have been obvious for a person of ordinary skill in the art to provide a separate non-volatile memory that is programmable after manufacturing for storing the user configuration data, since an MROM memory is only programmable during manufacturing. The motivation for doing so would be to allow the user to change the user-configuration of the programmable logic device after manufacturing, while leaving the self-test configuration data in the MROM since it does not need to be changed after initial design prototyping of the programmable logic device, thus realizing the combined advantage of allowing less costly mass production of MROMs for storing self-test configuration data and

realizing the advantage of allowing the user-configuration data to be programmable after manufacturing.

*Claim 11*

15. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Snowden et al. (combination F), as applied to claim 6 above.

The combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Snowden et al. (Combination F) has disclosed the steps of:

performing a self-test on a programmable logic circuit according to self-test configuration data in a self-test nonvolatile store (Stroud et al., discloses performing a self-test on the PLD, see col. 4, lines 25-38; The non-volatile storage means for storing the configuration data was provided by the serial configuration memory of Pathak et al., see rejection of claim 1 under 35 USC 103(a), combination B)

storing user configuration data in a user nonvolatile store if the programmable logic circuit passes the self-test. (*see*, Stroud et al., col. 2, lines 15-20, disclosing that the programmable logic device, i.e. FPGA, is temporarily programmed with test configuration data. This suggests that the FPGA is later reprogrammed for user configuration data.)

*Claim 12*

16. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Snowden et al. (combination E), as applied to claim 11 above, further in view of Pathak (US Patent 5,946,267) and Douskey et al. (US Patent 5,668,816).

The combination of Stroud et al., Kang et al., Pathak et al., Shyu and Snowden (Combination E) has disclosed that the self-test nonvolatile storage means is the same as the user nonvolatile storage means. (see rejection of Claim 1 under 35 USC 103(a), para. "Stroud et al. discloses...at least one storage device....that provides self-test configuration data...and can subsequently store user configuration data...").

Pathak et al. has disclosed that a serial configuration memory that can store a plurality of configurations at different addresses in the memory for the purpose of allowing quick reconfiguration of the FPGA, see col. 1, lines 55-58.

Combination G

At the time of invention if would have been obvious for a person of ordinary skill in the art to modify the combination of Stroud et al., Kang et al., Pathak et al., Shyu and Snowden (Combination E) such that the self-test configuration and the user configuration are stored at different location in the serial programmable memory as taught by Pathak et al..

The motivation for making this modification would be to allow for quick reconfiguration between the self-test mode and user-configuration mode.

Douskey et al. has taught that system testing is one of the most valuable assets of BIST to greatly enhance machine reliability. Every time a machine is powered on during a power-on-reset (POR) system test, the system can automatically run BIST to ensure all components are working properly. (col. 1, lines 34-38)

Combination H

At the time of invention if would have been obvious for a person of ordinary skill in the art to modify the combination of Stroud et al., Kang et al., Pathak et al., Shyu, Snowden, and Pathak et al. (Combination G) such that the self-test configuration is automatically loaded and executed after power-on-reset test, followed by loading the normal operating mode of the programmable logic device stored as the user configuration data. If the modification were made, the self-test configuration data would be load from the serial configuration memory at a predetermined address, followed by automatically loading the user configuration data from the serial configuration memory at a different predetermined address.

The motivation for making this modification would be to increase the reliability of the programmable logic device by automatically checking the device during power-on-reset testing of the device. (Douskey et al, col. 1, lines 34-38)

*Claims 9 and 10*

17. Claim 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Stroud et al., Kang et al., Pathak et al., Shyu, Snowden, and Pathak et al., and Douskey et al. (combination H), as applied to claim 12 above, further in view of Gill et al. (US Patent 5,032,533 A) . The combination of Stroud et al., Kang et al., Pathak et al., Shyu, Snowden, and Pathak et al., and Douskey et al. (combination H) has not explicitly disclosed that the non-volatile storage device includes at least two sectors and that self-test configuration data is stored in a first sector.

The combination of Stroud et al., Kang et al., Pathak et al., Shyu, Snowden, and Pathak et al., and Douskey et al. (combination H) has disclosed that the non-volitile memory is an EEPROM memory. (See rejection of claim 4, under 35 USC 103(a), para. "At the time of invention...").

From Gill et al., one of ordinary skill in the art would have recognized that flash memories are less expensive and higher capacity than EEPROM memories because memory cells are smaller and are not erased individually; and instead, the array of cells are erased in bulk. (Col. 1, lines 55-58)

Combination K

At the time of invention it would have been obvious for a person of ordinary skill in the art to modify the combination of Stroud et al., Kang et al., Pathak et al., Shyu, Snowden, and Pathak et al., and Douskey et al. (combination H) such that the EEPROM is replace by a Flash memory device that is functionally equivalent to the EEPROM device with the exception that the flash memory device is erased in blocks, i.e. sector of data at a time, where the suggestion of replacing the EEPROM with flash was provided by Gill et al.

The motivation for doing so would be to improve the memory capacity and lower the cost of the non-volatile memory. (Gill et al., col. 1, lines 55-58)

Combintation L

Further, at the time of invention it would have been obvious for a person of ordinary skill in the art to modify the combination of Stroud et al., Kang et al., Pathak et al., Shyu, Snowden, and Pathak et al., and Douskey et al., and Gill et al. such that each block of the flash, i.e. sector,

corresponds to a different configuration of the programmable logic device. This modification realizes as obvious the claim limitation that the non-volatile storage device includes at least two sectors (blocks). (Also, see, the rejection of claim 12, under 35 USC 103(a), combination G; "At the time of invention it would have been obvious....(to store) the self-test configuration and the user configuration .... at different location in the serial programmable memory").

The motivation for making this modification would be to simplify re-programming of a programmable logic configuration in the non-volatile memory by placing a single user configuration in each flash memory block (i.e. sector). Thus, realizing the advantage of allowing one programmable logic configuration to be reprogrammed without affecting the other logic configuration. (note, Gill et al. has taught that flash memories must be erased in blocks of data at a time, instead of individual cells at a time as is the case for EEPROM memories.)

Further, the combination of Stroud et al., Kang et al., Pathak et al., Shyu, Snowden, and Pathak et al., and Douskey et al., and Gill et al. has disclosed that the self-test configuration is automatically loaded and executed after power-on-reset test, followed by loading the normal operating mode of the programmable logic device stored as the user configuration data. (See obvious rejection of claim 12 under 35 USC 103(a), Combination H).

Combination M

At the time of invention it would have been obvious for a person of ordinary skill in the art to arrange the self-test configuration data as the first block (i.e. sector) in the non-volatile memory because this block is first loaded during power-on-reset testing.

The motivation for making this modification would be to simplify the implementation of the power-on-reset testing system by arranging blocks in the order that they are loaded from the memory.

This modification realizes as obvious the limitation of claim 9 that the self-test configuration data is loaded in to the sector of the non-volatile memory.

Also, This modification realizes as obvious the limitation of claim 10 that the first sector is the boot sector for the programmable logic device. It has been shown that it is obvious to "boot" the self-test from this sector during power-on-reset testing.

*Claim 13*

18. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Snowden et al., Pathak et al., and Douskey, (combination H) as applied to claim 12 above.

The combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Snowden et al., Pathak et al., and Douskey (Combination H) has disclosed that storing user configuration data includes programming user configuration data in locations that stored self-test configuration data. See Stoud et al., Col. 2, lines 54-55 disclosing that the FPGA is a re-programmable SRAM-based FPGA. Since the FPGA is SRAM based, when the user configuration data is load from the non-volatile memory, it must overwrite the self-test configuration data stored in the SRAM-cells internal to the FPGA. Thus, the user configuration data is programmed into the same SRAM-cells that previously held the self-test configuration.

*Claim 14*

19. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Snowden et al., Pathak et al., and Douskey, (Combination H) as applied to claim 13 above.

The combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Snowden et al., Pathak et al., and Douskey (Combination H) has disclosed that the user configuration data is programmed in locations that are different from those that store the self-test configuration data (*see*, Pathak et al., col. 1, lines 58-59, "each bitstream having it own beginning address").

*Claim 15*

20. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Snowden et al., Pathak et al., and Douskey, (combination H) as applied to claim 14 above.

The combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Snowden et al., Pathak et al., and Douskey (Combination H) has disclosed that the self-test nonvolatile storage means is formed on the same die as the programmable logic circuit. (see, rejection of claim 4 under 35 USC 103(a), combination H; Shyu et al. has taught the advantage of system-on-a-chip design.)

*Claim 16*

21. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Snowden et al., Pathak et al., and Douskey, (Combination H) as applied to claim 14 above, further in view of Tran (US Patent US 5909587 A).

The combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Snowden et al., Pathak et al., and Douskey (Combination H) disclosed assembling the programmable logic circuit on one die with the nonvolatile storage means on another die into one package.

The combination of Stroud et al., Kang et al., Pathak et al., Shyu, Snowden, and Douskey et al. (Combination H) has disclosed combining the programmable logic circuit and the non-volatile storage means into the same die and same package.

Tran has taught an old and well known concepts of system-on-a-chip design. Tran has taught that a system-on-a-chip design increases the die size; and that this increase in die size can result in difficulties in fabrication and in lower yields in manufacturing. One skilled in the art would have recognized that in order to mitigate this problem, one approach would be to separating the functional blocks within the system into smaller chips for incorporation within a multi-chip module. (col. 3, lines 1 to 13).

Combination I

At the time of invention it would have been obvious for a person of ordinary skill in the art to modifiy the combination of Stroud et al., Kang et al., Pathak et al., Shyu, Snowden, and Douskey et al. (Combination H) such that the non-volatile storage means and the programmable logic devices are split into separate dies and combined into one package as a multi-chip module, as suggested by Tran.

The motivation for make this modification would be to increase the manufacturing yield the system by converting from an system-on-a-chip package to a multi-chip module package. (See Tran)

*Claim 17*

22. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination Stroud et al., Kang et al., Pathak et al., Shyu, Snowden, Douskey et al., and Tran, (combination I) as applied to claim 16 above.

The combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Snowden et al., Pathak et al., Douskey, and Tran (Combination I) has disclosed one package that is a multi-chip module. (*see*, rejection of Claim 16 under 35 USC 103(a), combination I).

*Claim 18*

23. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination Stroud et al., Kang et al., Pathak et al., Shyu, Snowden et al., and Douskey, (combiation H) as applied to claim 12 above.

The combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Snowden et al., Pathak et al., and Douskey (Combination H) has disclosed the steps of:

storing self-test information in a first nonvolatile store, said information for placing said programmable logic circuit into a self-configuration (Stroud et al, col. 4, lines 25-31);

executing a self-test on the programmable logic circuit (Stroud et al, col 4, lines 31-38); and

providing user configuration information that places the programmable logic circuit in a user configuration (*see*, Stroud et al., col. 2, lines 15-20, disclosing that the programmable logic device, i.e. FPGA, is temporarily programmed. This suggests that the FPGA is later reprogrammed for user configuration data. Also, an FPGA is not useful unless it is eventually programmed with user configuration data. That is, programming the FPGA with only test configuration data and never loading user configurations is not a useful function for a FPGA.).

*Claim 19*

24. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination Stroud et al., Kang et al., Pathak et al., Shyu, Snowden et al., and Douskey, (combination H) as applied to claim 12 above.

The combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Snowden et al., Pathak et al., and Douskey (Combination H) has that the user configuration data is stored in the first nonvolatile store. (*see,* rejection of claim 12 under 35 USC 103(a), para. "At the time of invention....".)

*Claim 20*

25. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination Stroud et al., Kang et al., Pathak et al., Shyu, Snowden et al., and Douskey, (combination H) as applied to claim 12 above, further in view of Kraft et al. (US Patent 5,759,877).

The combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Snowden et al., Pathak et al., and Douskey (Combination H) has not disclosed that a second nonvolatile storage means is different from the first nonvolatile store.

The combination of Stroud et al., Kang et al., Pathak et al., Shyu, and Snowden et al., Pathak et al., and Douskey (Combination H) has disclosed that the non-volatile storage means is an EEPROM. (see rejection of claim 5 under 35 USC 103(a), para. "At the time of invention...").

Krafts et al. has taught that ROMs are useful wherever unalterable data ... are required because the data cannot be overwritten or otherwise altered by the user. A ROM is "programmed" during its manufacture by making permanent electrical connections in selected memory cells. (col. 1, lines 20-24).

Combination J

At the time of invention it would have been obvious for a person of ordinary skill in the art the modify the combination of Stroud et al., Kang et al., Pathak et al., Shyu, Snowden, and Douskey (combination H) such that it includes a separate PROM memory in addition to the EEPROM specifically for holding the self-test configuration data; and the EEPROM specifically for holding user configurations, where Kraft suggested using a PROM for storing data that should be protected from overwriting.

The motivation for doing so would be to prevent the self-test data from being overwritten unintentionally by the user when the user configuration data is programmed. This overwriting of the self-test configuration data would preclude the ability to automatically running the BIST during power-on reset (See Kraft, col. 1, lines 20-24; also, see obvious rejection of claim 12 under 35 USC 103(a), para. "Douskey et al. ...").

***Summary of Rejections***

26. The following is a summary of the standing for claims 1 to 20:

Claim 1 was rejected under 35 USC 103(a) over Combination B.
Claim 2 was rejected under 35 USC 103(a) over Combination B.
Claim 3 was rejected under 35 USC 103(a) over Combination C.
Claim 4 was rejected under 35 USC 103(a) over Combination D.
Claim 5 was rejected under 35 USC 103(a) over Combination E.
Claim 6 was rejected under 35 USC 103(a) over Combination E.
Claim 7 was rejected under 35 USC 103(a) over Combination F.
Claim 8 was rejected under 35 USC 103(a) over Combination N.
Claim 9 was rejected under 35 USC 103(a) over Combination M.
Claim 10 was rejected under 35 USC 103(a) over Combination M.
Claim 11 was rejected under 35 USC 103(a) over Combination F.
Claim 12 was rejected under 35 USC 103(a) over Combination H.
Claim 13 was rejected under 35 USC 103(a) over Combination H.
Claim 14 was rejected under 35 USC 103(a) over Combination H.
Claim 15 was rejected under 35 USC 103(a) over Combination H.
Claim 16 was rejected under 35 USC 103(a) over Combination H.
Claim 17 was rejected under 35 USC 103(a) over Combination I.
Claim 18 was rejected under 35 USC 103(a) over Combination H.
Claim 19 was rejected under 35 USC 103(a) over Combination H.
Claim 20 was rejected under 35 USC 103(a) over Combination J.

***Summary of Reference Combinations***

27. The following combination of references were made in formulating the rejection of claims 1 to 20 under 35 USC 103(a):

Combination A = Stroud et al. + Kang et al

Combination B = Combination A + Pathak et al.

Combination C = Combination B + Lawman

Combination D = Combination B + Shyu

Combination E = Combination D + Snowden et al.

Combination F = Combination D + Cook

Combination G = Combinaton E + Pathak et al.

Combination H = Combination G + Douskey .

Combination I = Combination H + Tran

Combination J = Combination I + Krafts

Combination K = Combination H + Gill et al.

Combination L = Combination K + Gill et al.

Combination M = Combination L + Gill et al.

***Conclusion***

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Patrick Moore whose telephone number is (703)305-9727. The examiner can normally be reached on 8:30 - 5 PM If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703)305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 746-7240.

William Patrick Moore
Examiner

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